Amendments to the Claims

The following Listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (withdrawn): A deposition system comprising:

an aperture mask including alignment edges and a deposition pattern defined in relation to the alignment edges; and

an alignment fixture including at least three contact points, wherein exactly three of the contact points contact the alignment edges of the aperture mask to align the pattern for a deposition process.

2. (withdrawn): The system of claim 1, wherein the pattern is defined in relation to the alignment edges such that, upon contact of the alignment edges with the contact points, the pattern is aligned to within a tolerance of less than approximately 10 microns.

3. (withdrawn): The system of claim 1, wherein the pattern defines at least a portion of an integrated circuit.

4. (withdrawn): The system of claim 1, wherein the aperture mask is formed from a silicon wafer.

5. (withdrawn): The system of claim 1, wherein the aperture mask is formed from a rigid polymer.

6. (withdrawn): The system of claim 1, wherein the alignment fixture further includes a securing element to secure the aperture mask in alignment.

7. (withdrawn): The system of claim 6, wherein the securing element includes a spring member that exerts a spring bias to force the aperture mask against the alignment fixture.

8. (withdrawn): The system of claim 1, further including a deposition substrate, wherein the deposition substrate includes alignment edges that substantially correspond to the alignment edges of the aperture mask, wherein the contact points contact the alignment edges of both the aperture mask and the deposition substrate such that the pattern is aligned for a deposition process onto the deposition substrate.

9. (withdrawn): A method comprising:

aligning a pattern of an aperture mask relative to a deposition substrate by positioning alignment edges of the aperture mask and deposition substrate in contact with exactly three contact points; and

depositing material onto the substrate through the pattern of the aperture mask.

10. (withdrawn): A method comprising:

forming a first pattern in a first mask substrate relative to alignment edges on the first mask substrate to define a first aperture mask;

aligning the pattern of the first aperture mask relative to a deposition substrate by positioning the alignment edges of the first aperture mask and alignment edges of the deposition substrate in contact with exactly three contact points; and

depositing material onto the deposition substrate through the pattern of the first aperture mask.

11. (withdrawn): The method of claim 10, further comprising:

forming a second pattern in a second mask substrate relative to alignment edges on the second mask substrate to define a second aperture mask;

aligning the pattern of the second aperture mask relative to the deposition substrate by positioning the alignment edges of the second aperture mask and the alignment edges of the deposition substrate in contact with exactly three contact points; and

depositing material onto the deposition substrate through the pattern of the second aperture mask.

12. (withdrawn): The method of claim 11, wherein the method is used in fabricating an integrated circuit.

13. (withdrawn): The method of claim 12, wherein the integrated circuit includes one or more complimentary transistor circuit elements.

14. (withdrawn): The method of claim 12, wherein the integrated circuit includes an organic semiconductor.

15. (withdrawn): The method of claim 12, wherein the integrated circuit includes an inorganic semiconductor.

16. (withdrawn): The method of claim 12, wherein the integrated circuit includes a layer of pentacene.

17. (withdrawn): The method of claim 12, wherein the integrated circuit includes a layer of amorphous silicon.

18. (withdrawn): The method of claim 12, wherein the material deposited onto the deposition substrate through the pattern of the first aperture mask forms a gate electrode, wherein the material deposited onto the deposition substrate through the pattern of the second aperture mask is a semiconductor, the semiconductor being deposited after the gate electrode is deposited, the method further comprising:

forming a third pattern in a third mask substrate relative to alignment edges on the third mask substrate to define a third aperture mask;

aligning the pattern of the third aperture mask relative to the deposition substrate by positioning the alignment edges of the third aperture mask and the alignment edges of the deposition substrate in contact with the exactly three contact points; and

depositing source and drain electrodes onto the semiconductor through the pattern of the third aperture mask.

19. (withdrawn): The method of claim 12, wherein the material deposited onto the deposition substrate through the pattern of the first aperture mask forms a gate electrode, wherein the material deposited onto the deposition substrate through the pattern of the second aperture mask forms a dielectric layer, the dielectric layer being deposited after the gate electrode is deposited, the method further comprising:

forming a third pattern in a third mask substrate relative to alignment edges on the third mask substrate to define a third aperture mask;

aligning the pattern of the third aperture mask relative to the deposition substrate by positioning the alignment edges of the third aperture mask and the alignment edges of the deposition substrate in contact with exactly three contact points; and

depositing a semiconductor onto the dielectric layer through the pattern of the third aperture mask;

forming a fourth pattern in a fourth mask substrate relative to alignment edges on the fourth mask substrate to define a fourth aperture mask;

aligning the pattern of the fourth aperture mask relative to the deposition substrate by positioning the alignment edges of the fourth aperture mask and the alignment edges of the deposition substrate in contact with exactly three contact points; and

depositing source and drain electrodes onto the semiconductor through the pattern of the fourth aperture mask.

20. (currently amended): An integrated circuit comprising:

a deposition substrate;

a patterned first electrode layer formed adjacent the deposition substrate;

a patterned organic semiconductor layer formed adjacent the first electrode layer; and

a second patterned electrode layer deposited adjacent the organic semiconductor layer, wherein the patterned first electrode layer, the patterned organic semiconductor layer, and the second patterned electrode layer are each defined by a repositionable aperture mask, and wherein

one of the patterned first electrode layer and the patterned second electrode layer defines source and drain electrodes, and one of the patterned first electrode layer and the patterned second electrode layer defines a gate electrode.

21. (original): The integrated circuit of claim 20, wherein the patterned first electrode layer defines a gate electrode, and wherein the second patterned electrode layer defines source and drain electrodes.

22. (original): The integrated circuit of claim 20, wherein the patterned first electrode layer defines source and drain electrodes, and wherein the patterned second electrode layer defines a gate electrode.

23. (original): The integrated circuit of claim 21, wherein the source and drain electrodes are separated by a gap less than approximately 20 microns.

24. (original): The integrated circuit of claim 23, wherein the gap is less than approximately 10 microns.

25. (original): The integrated circuit of claim 20, wherein the organic semiconductor comprises a polycrystalline organic semiconductor.

26. (original): The integrated circuit of claim 25, wherein the organic semiconductor is pentacene.

27. (original): The integrated circuit of claim 20, further comprising one or more complimentary transistor circuit elements.

28. (original): The integrated circuit of claim 27, wherein the complementary transistor circuit elements include a semiconductor layer comprising amorphous silicon.

29. (original): The integrated circuit of claim 20, wherein one or more of the layers include one or more interconnects.

30. (original): The integrated circuit of claim 20, further comprising one or more interconnect layers.

31. (original): The integrated circuit of claim 30, wherein the interconnect layers are defined by one or more repositionable aperture masks.

32. (original): The integrated circuit of claim 20, further comprising a patterned dielectric layer formed adjacent the organic semiconductor layer.

33. (original): The integrated circuit of claim 20, wherein the integrated circuit forms at least part of a circuit selected from the following group of circuits: an electronic display, a radio frequency identification (RFID) circuit, and an electronic memory.

34. (withdrawn): A transistor comprising:

a first patterned conductive layer;

a patterned dielectric layer formed over the deposited conductive layer;

a patterned organic semiconductor layer formed over the deposited dielectric layer; and

a second patterned conductive layer formed over the deposited organic semiconductor layer, wherein each patterned layer is defined by a repositionable aperture mask.

35. (withdrawn): The transistor of claim 34, wherein the second deposited conductive layer defines source and drain electrodes separated by a gap less than approximately 20 microns.

36. (withdrawn): The transistor of claim 34, wherein the transistor forms at least part of a radio frequency identification (RFID) circuit.

37. (withdrawn): The transistor of claim 35, wherein the gap is less than 10 microns.

38. (withdrawn): An aperture mask comprising:

a crystalline wafer; and

apertures formed in the crystalline wafer and defining straight edges, wherein the straight edges of the apertures are not aligned with cleavage planes of the crystalline wafer.

39. (previously presented): The integrated circuit of claim 20 wherein at least one of said first electrode layer, said patterned organic semiconductor layer or said second patterned electrode layer is vapor deposited.

40. (previously presented): The integrated circuit of claim 20 wherein each of said first electrode layer, said patterned organic semiconductor layer or said second patterned electrode layer are vapor deposited.